

**Page 6, first full paragraph:**

According to this invention, a computer software product for calculating pin-to-pin delay time  $T_{\text{iopath\_aged}}$  and block-to-block delay time  $T_{\text{iopath\_aged}}$  is provided. The pin-to-pin delay time  $T_{\text{iopath\_aged}}$  is delay time of a signal passing between an input pin and an output pin of a logic block. The block-to-block delay time  $T_{\text{connect\_aged}}$ , which is delay time of a signal passing between said two logic blocks connected to each other in a computer. And then, the computer software product makes a computer execute the following processes:

**IN THE CLAIMS:**

**Please cancel claims 1 and 7 without prejudice or disclaimer.**

**Please enter the following amended claims:**

2. (Twice Amended) A method of calculating, by the use of a computer, a numerical value  $V_A$  representative of a circuit property of a logic level circuit, from a numerical value  $V_B$ , which shows a block property of a logic block included in the logic level circuit, the method comprising:

(a) calculating the value  $V_B$  from a plurality of numerical values  $V_C$ , each value  $V_C$  representing a transistor property of a transistor included in the logic block; and,

(b) calculating the value  $V_A$  from the value  $V_B$ , and outputting the value  $V_A$  as a value representative of a circuit property of said logic level circuit

, wherein, in the step (a), the plurality of values  $V_C$  comprises a first group of  $V_C$  values of transistors connected directly to an input pin of the logic block and a second group of  $V_C$  values of transistors connected directly to an output pin of the logic block.

3. (Twice Amended) A method of calculating, by the use of a computer, a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, comprising:

(a) calculating the pin-to-pin delay time, based on a value  $V_C$  of a transistor property of a transistor included in the logic block, and the block-to-block delay time without calculating in aging caused by hot carrier effect;

(b) calculating variations of signal delay times caused by aging, based on the value  $V_C$  of a transistor connected to the input pin and the value  $V_C$  of a transistor connected to the output pin; and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit.

4. (Twice Amended) A method of calculating, by the use of a computer, pin-to-pin delay time  $T_{iopath\_aged}$ , which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time  $T_{connect\_aged}$ , which is delay time of a signal passing between said two logic blocks connected to each other, comprising:

(a) calculating an amount of stress  $S_{in}$  cast by the input pin and an amount of stress  $S_{out}$  cast by the output pin according to the following expression:

$$S = \alpha \left( \frac{C}{W} \right)^\beta$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by  $\alpha$  and  $\beta$ , and width of channel of the transistor connected to the pin is represented by W [ $\mu\text{m}$ ];

(b) calculating an aged delay time of the input pin  $\delta_{\text{in}}$  [%] and an aged delay time  $\delta_{\text{out}}$  [%] according to the following expression:

$$\delta = \gamma \left( \frac{\tau S f}{\varepsilon_1 e^{\kappa T}} \right)^{\frac{1}{\varepsilon_2}}$$

where a constant depending on physical structure of the pin is represented by  $\gamma$ , the term of guarantee of the LSI is represented by  $\tau$  [hour], constants depending on process are represented by  $\varepsilon_1$ ,  $\varepsilon_2$  and  $\kappa$ , working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of said logic level circuit the pin-to-pin delay time  $T_{iopath\_aged}$  and the block-to-block delay time  $T_{connect\_aged}$  according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh} (1 + \lambda_{in} \delta_{in} + \lambda_{out} \delta_{out})$$
$$T_{connect\_aged} = T_{connect\_fresh} (1 + \lambda_{out} \delta_{out})$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by  $T_{iopath\_fresh}$  [ps] and  $T_{connected\_fresh}$  [ps], and ratios of delay times occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by  $\lambda_{in}$  and  $\lambda_{out}$ .

8. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating a numerical value  $V_A$ , which shows a property of a logic level circuit, from a numerical value  $V_B$ , which shows a property of a logic block constituting the logic level circuit, the program making a computer execute the following processes:

(a) calculating the  $V_B$  value from a plurality of numerical values  $V_C$ , each  $V_C$  value showing a property of a transistor constituting part of the logic block; and,

(b) calculating the  $V_A$  value from the  $V_B$  value, and outputting the  $V_A$  value for use as a value representative of a circuit property of said logic level circuit,

wherein in process (a) the plurality of  $V_C$  values comprises a  $V_C$  value of a transistor connected directly to an input pin of the logic block and another  $V_C$  value a transistor connected directly to an output pin of the logic block.

9. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating a delay time of a signal passing through a logic level circuit which includes a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, the program making a computer execute the following processes:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect;

(b) calculating variations of signal delay times caused by aging, based on values for the transistors connected directly to the input and output pins of logic blocks ; and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit.

10. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating pin-to-pin delay time  $T_{iopath\_aged}$ , which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time

Tconnect\_aged, which is delay time of a signal passing between said two logic blocks connected to each other by a computer, the program making a computer execute the following processes:

(a) calculating an amount of stress Sin cast by the input pin and an amount of stress Sout cast by the output pin according to the following expression:

$$S = \alpha \left( \frac{C}{W} \right)^{\beta}$$

4  
B  
SC  
where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by  $\alpha$  and  $\beta$ , and width of channel of the transistor connected to the pin is represented by W [ $\mu\text{m}$ ];

(b) calculating an aged delay time of the input pin  $\delta_{in}$  [%] and an aged delay time  $\delta_{out}$  [%] according to the following expression:

$$\delta = \gamma \left( \frac{\tau S f}{\epsilon_1 e^{\kappa T}} \right)^{\frac{1}{\epsilon_2}}$$

where that a constant depending on physical structure of the pin is represented by  $\gamma$ , the term of a guarantee of the LSI is represented by  $\tau$  [hour], constants depending on process are represented by  $\epsilon_1$ ,  $\epsilon_2$  and  $\kappa$ , working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of said logic level circuit the pin-to-pin delay time  $T_{iopath\_aged}$  and the block-to-block delay time  $T_{connect\_aged}$  according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh} (1 + \lambda_{in} \delta_{in} + \lambda_{out} \delta_{out})$$
$$T_{connect\_aged} = T_{connect\_fresh} (1 + \lambda_{out} \delta_{out})$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by  $T_{iopath\_fresh}$  [ps] and  $T_{connected\_fresh}$  [ps], and ratios of delay times occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by  $\lambda_{in}$  and  $\lambda_{out}$ , respectively.

11. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the program as in claim 9; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

12. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the program as in claim 10; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

**Please add the following new claims:**

13. (New) A signal delay calculation system which calculates the delay time of a signal passing through a logic level circuit consisting of a plurality of logic blocks, the system comprising:

first calculation means for calculating value  $V_B$ , a property of a logic block constituting the logic level circuit, based on a plurality of numerical values  $V_C$ , the  $V_C$  value representing a property of a transistor included in the logic block;

second calculation means for calculating a value  $V_A$  representing a signal delay property of a logic level circuit, from value  $V_B$ ; and

output means for outputting value  $V_A$ ,

wherein in the first calculation means, the plurality of  $V_C$  values includes exclusively a  $V_C$  value of a transistor connected directly to an input pin of the logic block and a  $V_C$  value of a transistor connected directly to an output pin of the logic block.



14. (New) The system of claim 13, wherein  $V_A$  is an aging delay property of a logic level circuit.